Name: Ningyuan Zhang

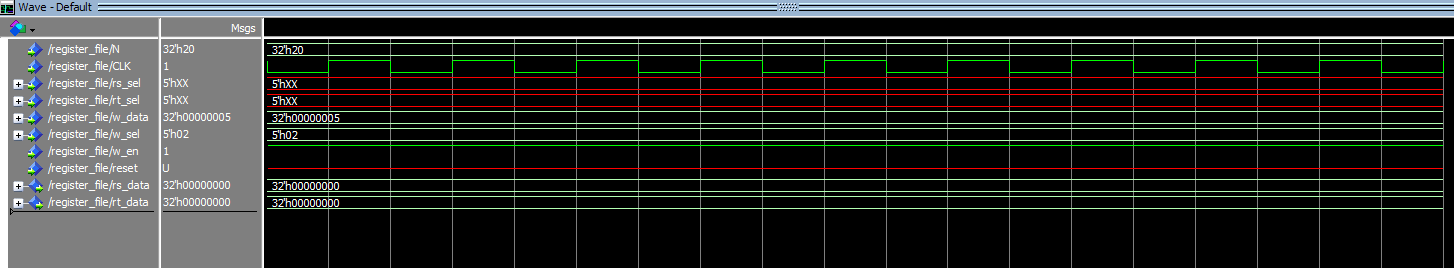
Section: A

Date: 3/8/2017

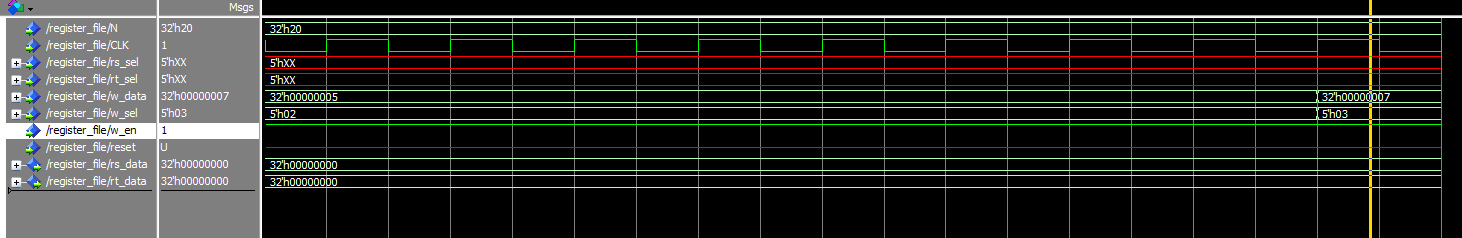
Instructor: Akhilesh Tyagi

Lab-7

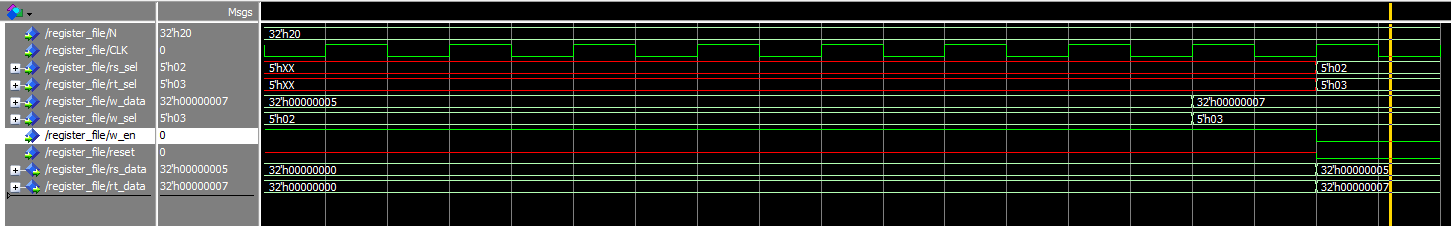
1). reg file:



write 5 into r2



write 7 into r3



read 5 from r2 and 7 from r3

2). ALU:

0000 add

0001 sub

0010 xor

0011 nor

0100 nand

0101 and

0110 or

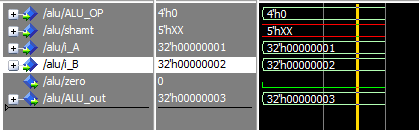
0111 slt

1000 mult

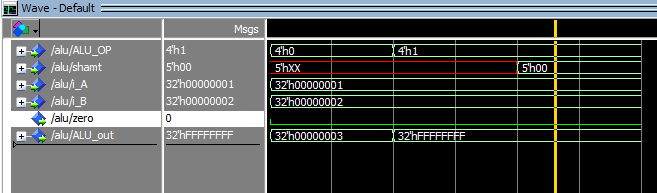
1001 sra

1010 srl

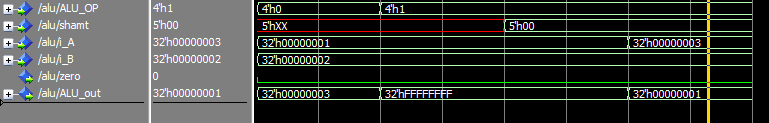
1011 sll



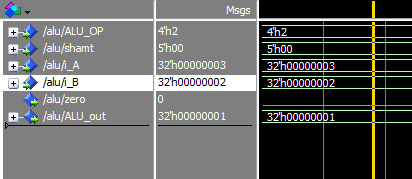
add 1+2



sub 1-2



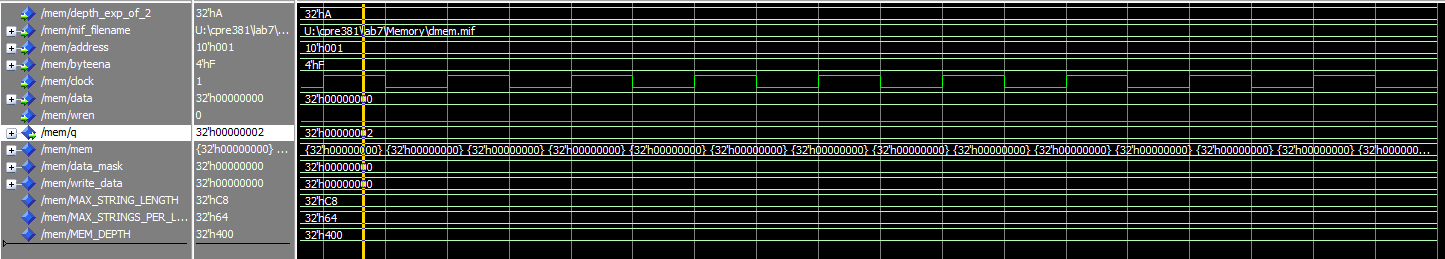
sub 3-2



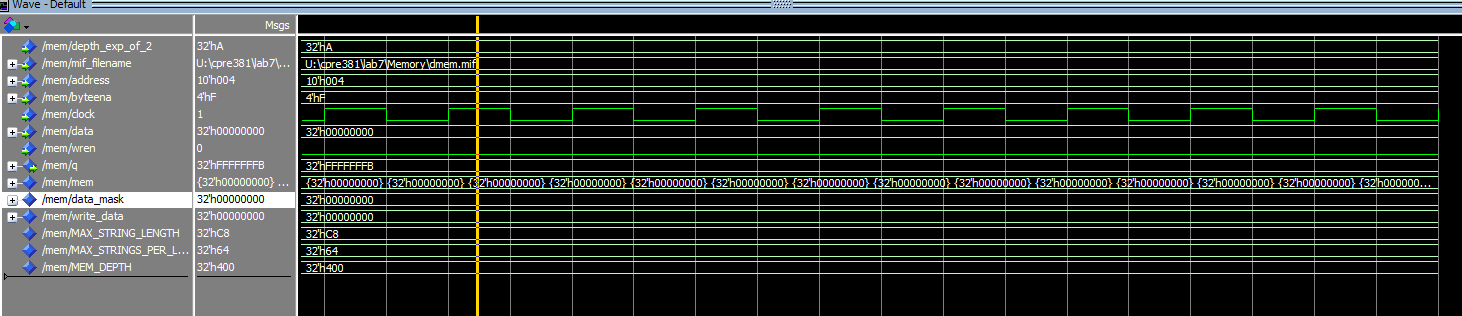
xor 3xor2

3). mem:

dmem.mif had been modified in folder memory



value in addr 1



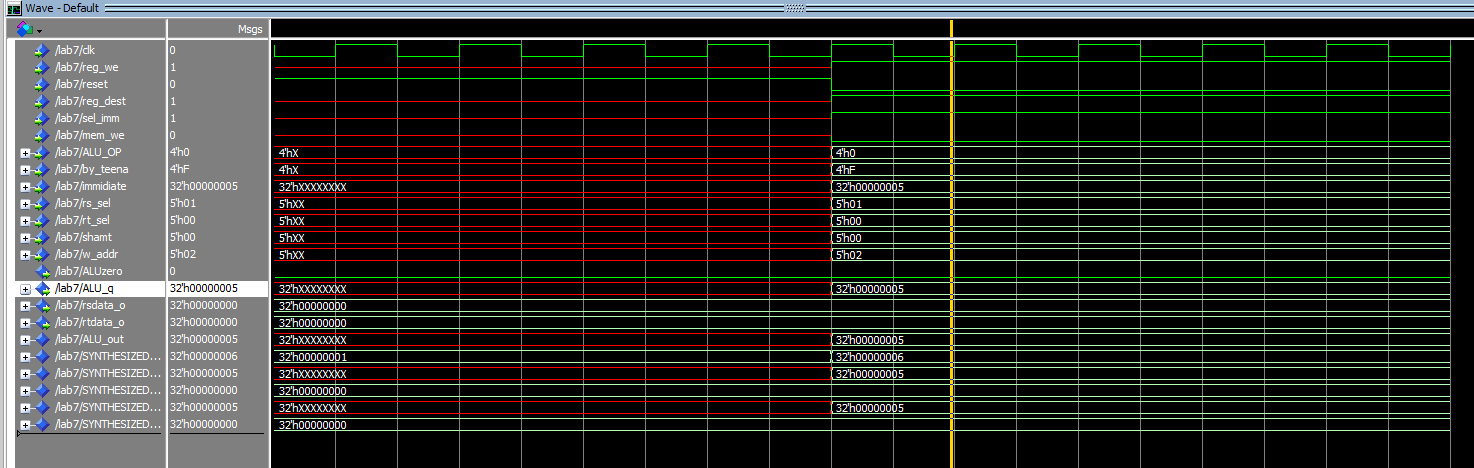
value in addr 4

4). mips processor

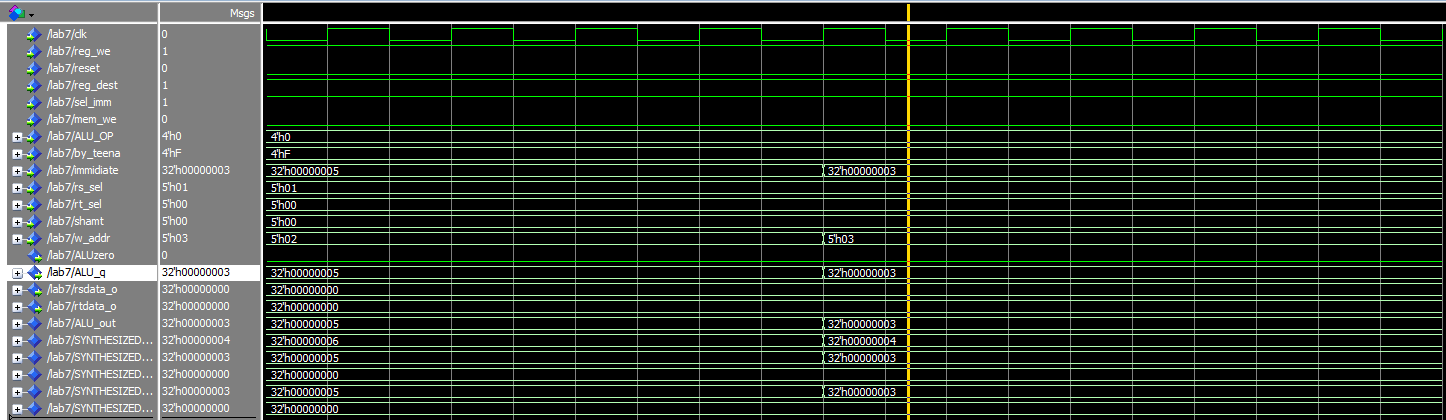
block diagram was saved as lab7.bdf

vhdl file was named as lab7.vhd

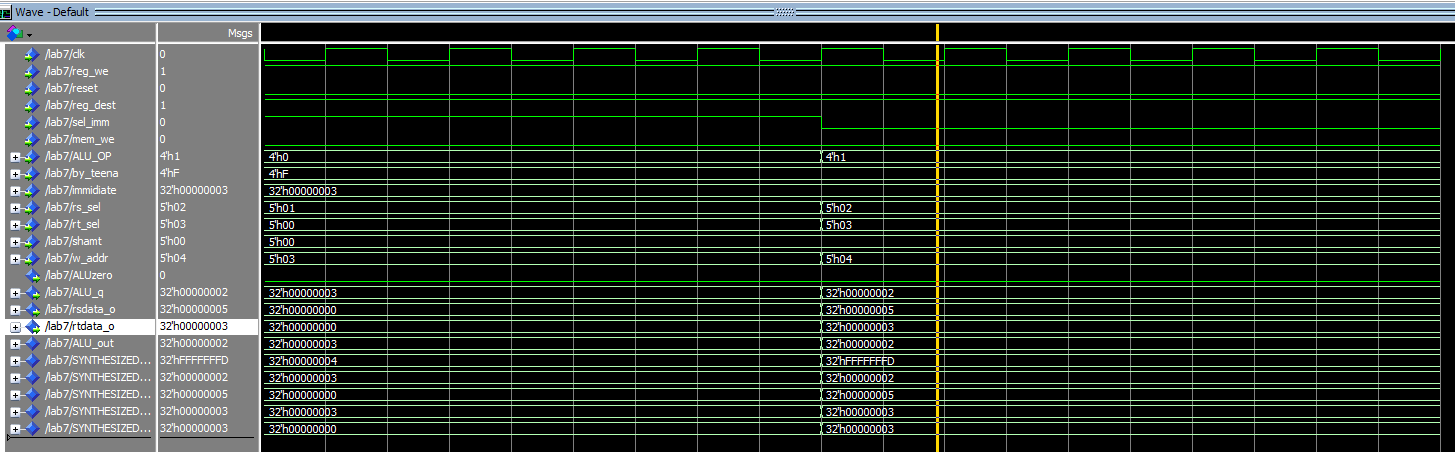
(after reset all registors are 0)



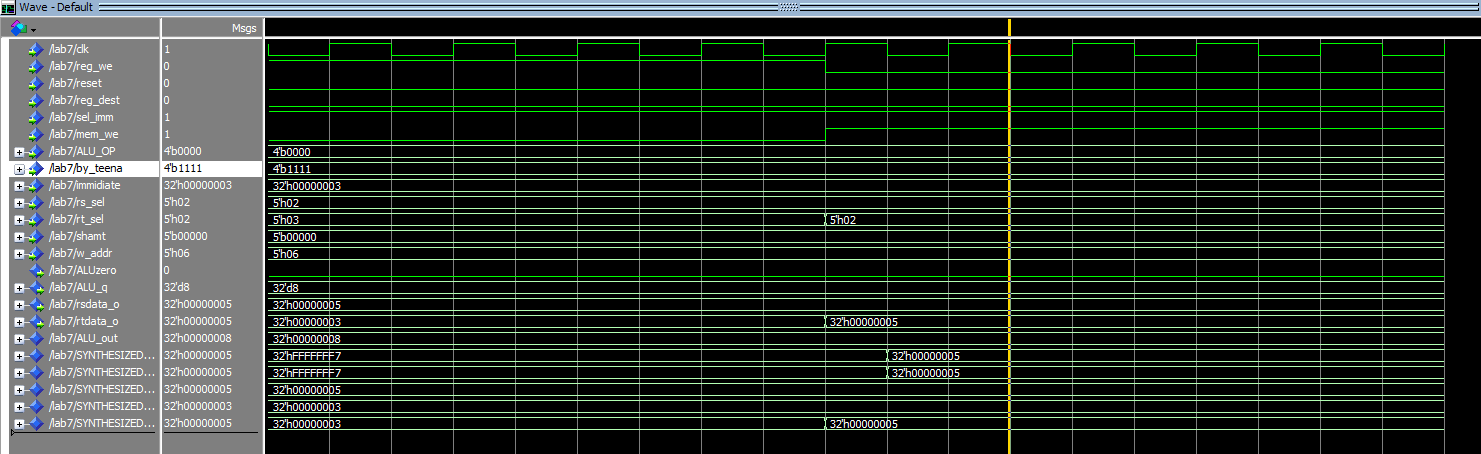
addi r2,r1,5



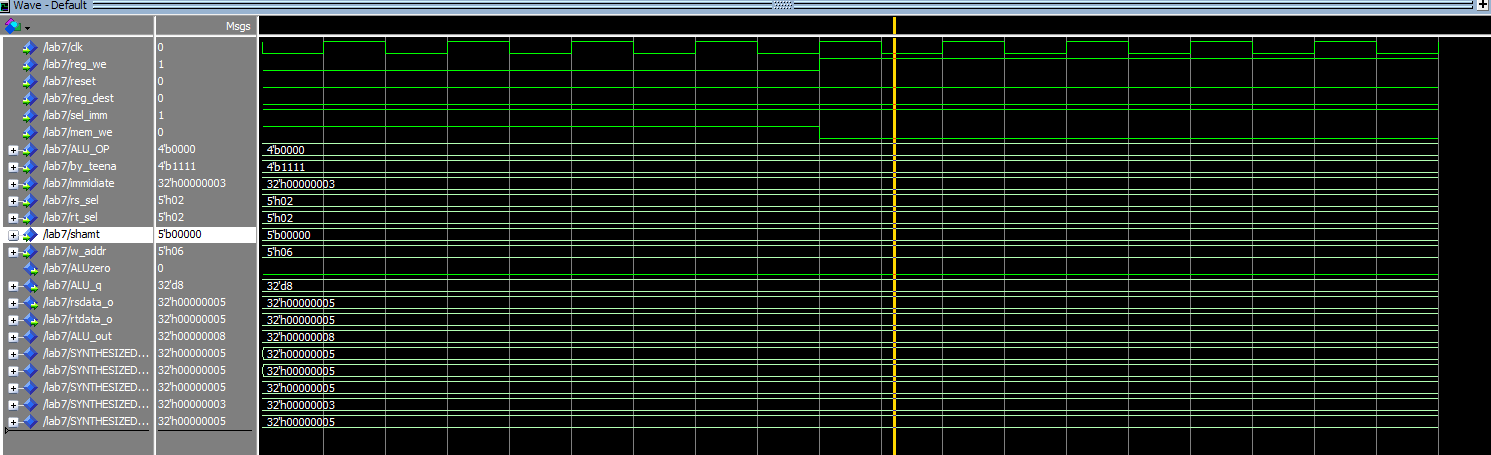
addi r3,r1,3



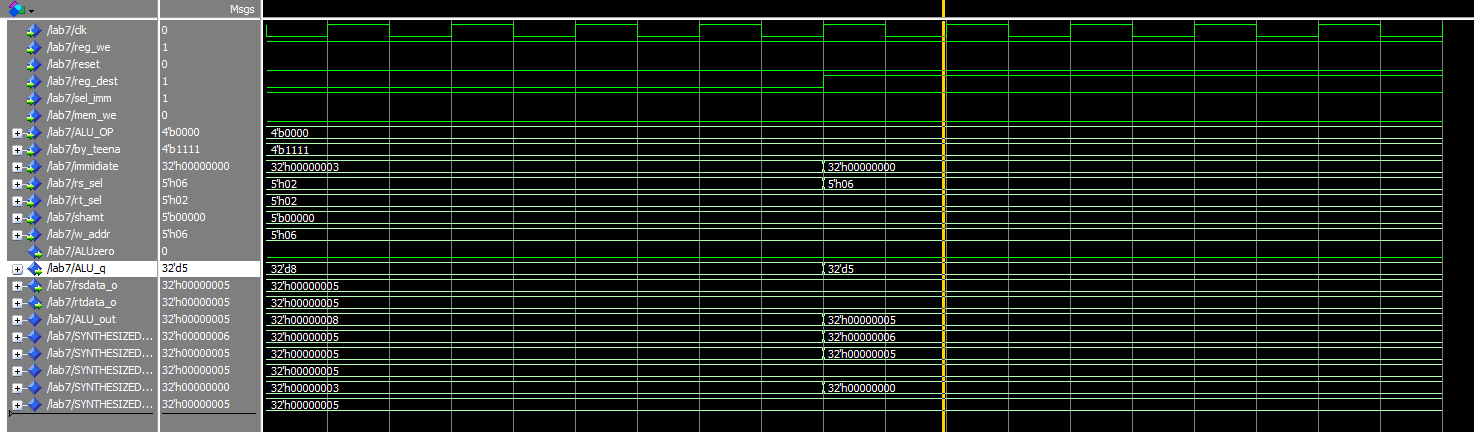
sub r4,r2,r3



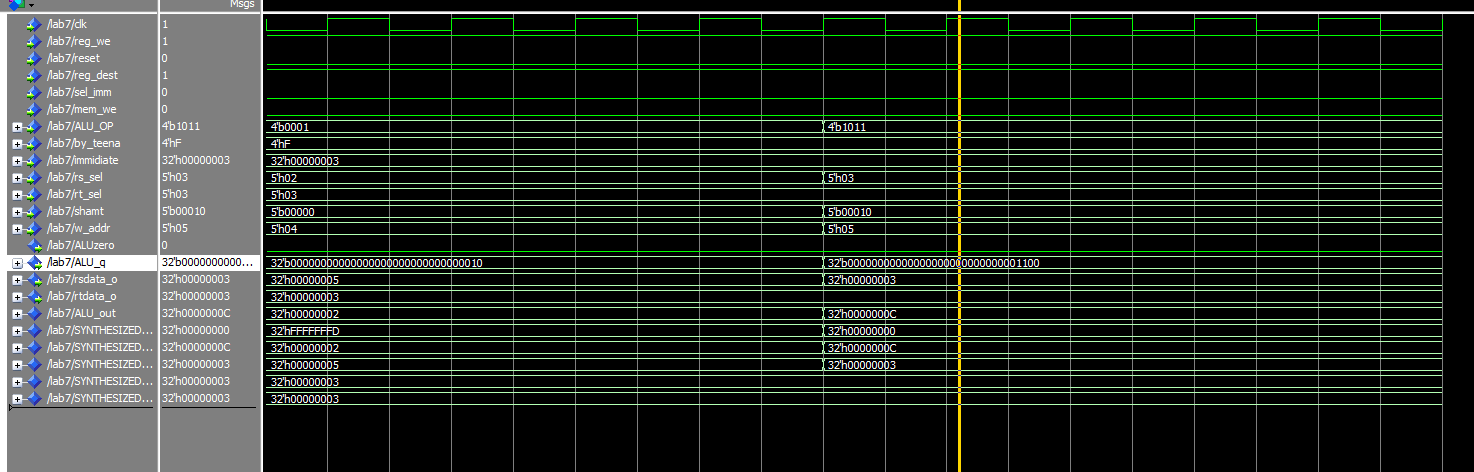
sw r2,3(r2)



lw r6,3(r2)

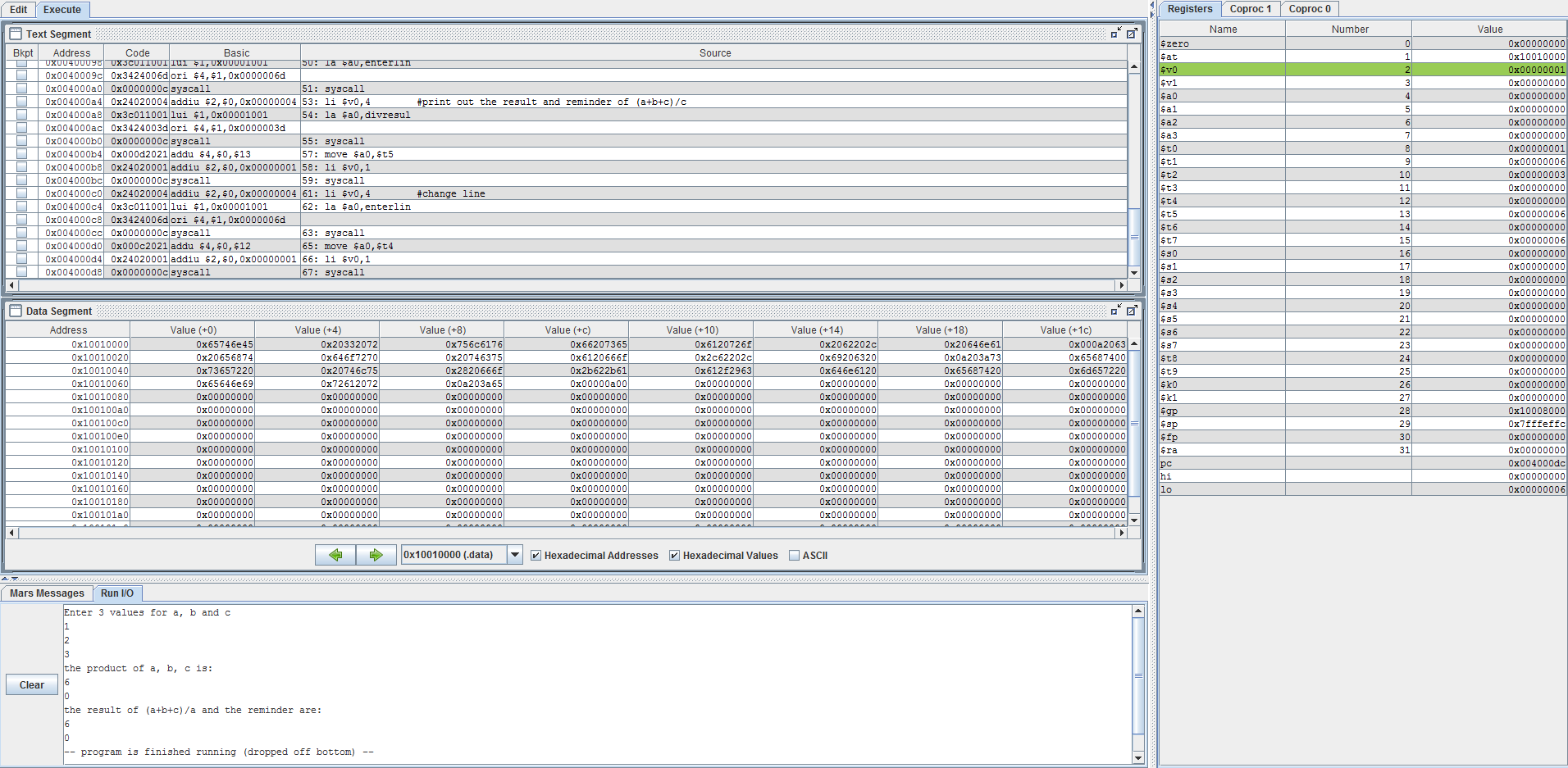


check sw, lw in r6



sll r5,r3,2

5). hi and lo reg



file name is b1.s

6). floating point arithmetic

file name is b2.s

